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09/244,788	02/05/99	PARIKH S	002818/PDD/P

EXAMINER	
PHAM, T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/244,788	PARIKH, SUKETU A.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *33-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2, 4-7* .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-32 in Paper No. 9 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1 line 10, "the first etch mask" lacks of antecedent basis

In claims 1 lines 6 and 15, claim 14 lines 2 and 4, claim 19 lines 7, 9, 21 and 23, the use of term "predetermined" reads on a nebulous mental step conducted prior to the manipulative steps of the claimed process, hence rendering the present process claim unclear in meaning in scope. If applicant wishes to patent detail controls over the recited process, then the process steps must be positively recited. *See* Seagram & Sons Inc. vs. Marzall, 84 USPQ

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-5, 7-9, 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Inohara et al [US 5,976,972].

Inohara et al, figs 8-49 col 1-19 particularly embodiment of figs 28-32, discloses the claimed method of forming a structure on a substrate comprising steps of:

depositing a first dielectric layer (43, Silicon oxide containing C, fig 28) on a substrate wherein a cap layer (54, fig 28) interposed between the substrate and the first dielectric layer;

depositing a second dielectric layer (44, SiN, fig 28) on the first dielectric layer;

depositing a first mask layer on the second dielectric layer wherein the first mask layer including a first via pattern having a width T, anisotropically etching the first via pattern (51, fig 28) through the second dielectric layer, and removing the first mask layer [see col 13 lines 20-24 for details]

depositing a third dielectric layer (45, Silicon oxide containing C, fig 29) on the second dielectric layer;

depositing a second mask (47, fig 29) on the third dielectric layer wherein the second mask includes a trench pattern overlaying the first via pattern and having a width P, such that

T exceeds P by a measure M, whereby the first via pattern and the trench pattern are adapted for fabricating a dual damascene structure;

anisotropically etching the first trench pattern through the third dielectric layer thereby forming a trench and a second via pattern, and anisotropically etching the second via pattern through the first dielectric layer thereby forming a via hole extending to a substrate [see fig 31 col 13 lines 39-53]; and

filling the trench and via hole with a conductive material (49, Al-Cu, fig 32) thereby forming a dual damascene structure (491-492, fig 32)

With respect to claim 4, Inohara et al teaches anisotropically etching the trench through the second dielectric (44) and simultaneously anisotropically etching the via hole through the cap layer (54, fig 31)

4. Claims 13, 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Inohara et al [US 5,976,972].

Innohara et al, figs 35-40 col 14 lines 30-67 and col 15, discloses the claimed method of forming a structure on a substrate comprising steps:

forming a dielectric stack (54, 43, 44, fig 37) including an etchstop layer (44, SiN);

forming a sacrificial etch segment, a first trench and a second trench on the etch stop [the sacrificial etch segment, first trench and second trench are located in the split region 51 in fig 39] such that the sacrificial etch segment is position between the first and second trenches;

forming a first via hole underlying the first trench such that the first via hole communicates the first trench, forming a second via hole underlying the second trench such that the second via hole communicate the second trench, wherein: (1) the first trench and the

first via hole, and (2) the second trench and the second via hole are adapted for forming a first dual damascene structure and a second dual damascene structure respectively [see figs 35-36 and 40 for details]; and

filling the first and second trenches, and the first and second via holes with conductive material (49, Al-Cu, fig 40) whereby the first and second dual damascene structure are formed.

5. Claims 13-14, 16-23, and 28-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin [US 6,093,632].

Lin, figs 4-8 col 1-6, discloses the claimed method of forming a structure on a substrate comprising steps of:

depositing a first dielectric (4, silicon oxide, fig 4) on a substrate wherein a cap layer (3, fig 4) interposed between the substrate and the first dielectric layer;

depositing a second dielectric layer (10a, SiN, 4) on the first dielectric layer;

depositing a first mask layer (11, fig 5) on the second dielectric layer wherein the first mask layer includes: (1) a first via pattern having a width T, (2) a second via pattern and (3) a sacrificial etch pattern position between the first and second via patterns such that the sacrificial etch pattern has a width W;

anisotropically etching the first and second via patterns through the second dielectric layer and forming a sacrificial etch segment by simultaneously anisotropically etching the sacrificial etch pattern through the second dielectric layer [see fig 5-6];

removing the first mask layer;

depositing a third dielectric layer (13, silicon oxide, 6) on the second dielectric layer;

depositing a second mask (14, fig 6) on the third dielectric layer, wherein the second mask includes: (1) a first trench pattern with a width P overlaying the first via pattern and the third dielectric layer , and (2) a second trench pattern overlaying the second via pattern and the third dielectric layer, and having a distance D between the first and second trench patterns wherein D exceed W by a measure N, in which: (1) the first via pattern and the first trench pattern are adapted for forming a first dual damascene structure and (2) the second via pattern and the second trench pattern are adapted for forming a second dual damascene structure;

anisotropically etching the first and second trench patterns through the third dielectric layer thereby forming a first trench and a second trench, additionally forming a third and fourth via pattern;

anisotropically etching the third and fourth via patterns through the first dielectric layer thereby forming a first via hole and a second via hole [see 7 col 5 lines 54-67 and col 6 lines 1-8]; and

filling the first trench, the first via hole, the second trench and the second via hole with conductive material (Cu, fig 8) whereby first and second dual damascene structures are formed.

With respect to claims 22, Lin teaches anisotropically etching the first and second trenches through the second dielectric layer and simultaneously anisotropically etching the first and second via holes through the cap layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 7, 10, 15, 24-27 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin [US 6,093,632] in the view of Inohara et al [US 5,976,972].

With respect to claim 31, Lin fails to teach the width T of the first via pattern exceeding the width P of the first trench pattern by a measure M.

However, Inohara et al teaches that forming a dual damascene structure with the width T of the first via pattern exceeding the width P of the first trench pattern by a measure M will provide better connection (communication) between the first trench and the first via hole in interconnect -- since an allowance for an alignment error between upper and lower wiring elements (in the first trench and the first via hole respectively) is provided thereby the area contact between the upper and lower wirings is not deteriorate due to misalignment [see Inohara et al col 12 lines 60-67 and col 13 lines 1-3].

Therefore, it would have been obvious for those skilled in the art to combine the teaching of Inohara et al in the process of Lin to make the width T of the first via pattern exceeding the width P of the first trench pattern by a measure M for making a better dual damascene structure with reasons given above.

With respect to claims 7, 10, 25 and 27, amorphous fluorinated carbon, organic SOG, SOG, aero-gel, polyarylene ethers, fluorinated polyarylene ether, divinyl siloxane benzocyclobutane, and Black Diamond™ are well-known low-k dielectric materials. It would have been obvious for those skilled in the art to use any of these material in the process of Lin and/or Inohara et al to make a dual damascene structure – since it has been well-known in the art that these materials can provide a good dual damascene structure with a decreased capacitance for a better interconnection in a semiconductor device.

With respect to claims 6, 15, 24 and 32, ranges values of measure M and measure N are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *In re Aller 105 USPQ233, 255 (CCPA). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA*

1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time of invention was made would have used any suitable range of N or M in the process of Lin and/or Inohara et al in order to optimize the process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (703) 308-6172. The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bowers Charles can be reached on (703) 308-2417. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-3432 for regular communications and (703) 308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thanhha Pham
January 9, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800